

MONOLITHIC HEMT LNAS FOR RADAR, EW, AND COMM

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ABSTRACT

Several monolithic HEMT low noise amplifiers (LNAs), designed for 7-11 GHz airborne radar, 2-18 GHz electronic warfare, and 20 GHz military satellite communications applications have demonstrated outstanding performance. Two-stage MMICs achieve as low as 1.2 dB noise figure at 10 GHz with 15 dB gain, and typically less than 1.8 dB noise figure from 7-11 GHz. A distributed amplifier demonstrates 3.0-5.2 dB noise figure with around 11 dB gain from 2-18 GHz. Finally, a three-stage MMIC achieves less than 2.0 dB noise figure from 18-23 GHz with 29 dB associated gain, representing the highest level of performance yet reported for a low-noise MMIC.

INTRODUCTION

The requirements for advanced radar, EW, and communications systems place stringent requirements on their microwave components. High dynamic range, low noise amplifiers are important components in all these systems. For example, X-Band T/R modules for airborne phased arrays operating across bandwidths up to 40% require LNAs with less than 2.5 dB noise figure, together with good gain, VSWR, and third order intercept performance. Similar low-noise amplifier requirements exist for EW receiver systems, with added emphasis on bandwidth to counter potential threats across the frequency spectrum [1]. For satellite communications (SATCOM) bands where operation has moved to 20, 44, and 60 GHz, high dynamic range amplifiers will be required for EHF ground terminals, and future airborne and spaceborne

conformal phased arrays [2]. The development of high electron mobility transistor (HEMT) monolithic microwave integrated circuits (MMICs) is progressing rapidly in response to these and other systems requirements [3-7].

MMICs are expected to improve the size, weight, reliability, and cost factors over many hybrid systems architectures, and HEMT MMICs have already demonstrated superior low-noise and high gain performance to their MESFET counterparts. However, integration of the HEMT device into MMICs still poses several processing challenges if these circuits are to become affordable. The objective of this work was to develop HEMT low noise amplifier circuits for multiple applications, using both 0.5 and 0.25 micron gate lengths, that demonstrate not only the performance advantage of HEMT MMICs over MESFETs but address the low cost fabrication issues as well. Three circuits have been developed: a two-stage feedback amplifier at X-Band, using a 0.5 micron combined optical stepper and E-beam lithographic process; a 2-18 GHz distributed amplifier, and a three-stage 20GHz amplifier both using 0.25 micron direct write E-beam lithography.

X-BAND HEMT MMIC

A two-stage circuit, shown in Figure 1, was designed to be used in an advanced T/R module for X-Band phased array antennas. The requirements are for low noise figure--less than 2.5 dB, with good input and output return losses over a 40% bandwidth at X-Band.

Several design tradeoffs exist between noise figure, input match, and gain for a given

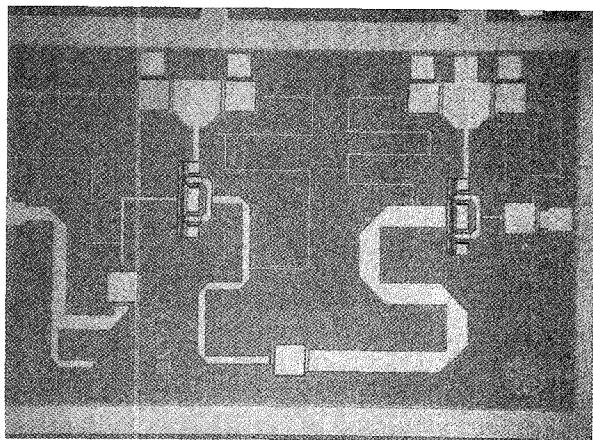


Figure 1. Two-stage X-Band HEMT MMIC. (Chip size: $0.063 \times 0.100 \text{ in}^2$.)

bandwidth. Input match and gain can be improved at the expense of noise figure; gain flatness and good noise figure can be achieved at the expense of input match. The use of series feedback between the source of the transistor and ground provides a means of improving input match while maintaining good noise figure performance. Additionally, the stability of the transistor is improved within the required frequency band, although out-of-band stability must be checked. The amount of feedback employed in this design was optimized to ensure that the complete amplifier had the overall performance of good noise figure, good input/output matches, sufficient gain over the bandpass frequency of 7-11 GHz, and unconditional stability over the analyzed frequency range of 5 MHz to 50 GHz.

The two-stage amplifier uses new 0.5×300 micron devices that include airbridges to enable source grounding from one side of the transistor, thereby reducing circuit size. In the absence of any 0.5×300 micron HEMTs to measure, S-parameters and noise parameters were estimated based on measurements made on similar devices. Accurate noise figure parameters were generated from the HEMT equivalent circuit model, using a modified Podell noise model [8]. The model is modified by reducing the value of the gate and intrinsic input resistances until the Podell model more closely corresponds to measured minimum noise figure. The minimum noise figure, F_{min} , of the HEMT is approximately 0.9 dB at 10 GHz.

The matching circuit topologies used for the input, inter-stage, and output use distributed microstrip transmission line elements and incorporate MIM capacitors for DC blocking. The devices are passivated with silicon nitride during capacitor formation. The amplifier chip is 0.063 in. wide by 0.100 in. long and 0.004 in. thick.

Typical performance, shown in Figure 2, indicates a measured noise figure of less than 1.8 dB across the 7-11 GHz frequency range and less than 1.5 dB from 8-10.5 GHz. The lowest noise figure measured for this circuit was at 9 GHz with 1.35 dB and 15.5 dB associated gain. Other circuits exhibit similar characteristics, presented in Table 1, the best showing 15 dB gain with 1.2 dB noise figure at 10 GHz.

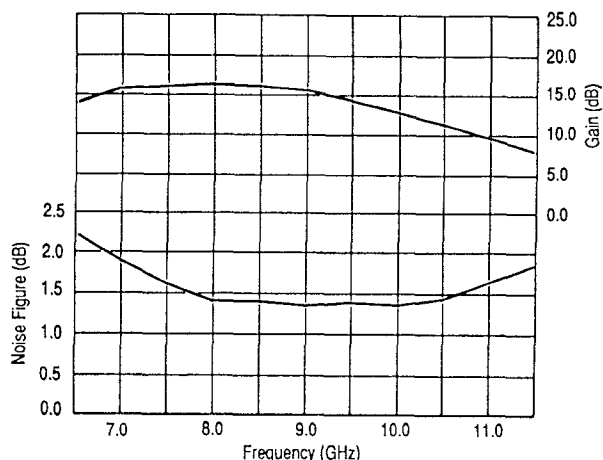


Figure 2. Measured Performance of X-Band HEMT MMIC

The worst case input and output return losses of the circuits were measured to be 4 dB and 11.5 dB, respectively, across the band 7-11 GHz. The gain compression, third order intercept and DC turn on time were also measured for this circuit. At 9 GHz, the measured output power at 1 dB gain compression was 12.5 dBm with minimum of +21 dBm third order intercept point. The DC turn on time, to quiescent power out, was less than 40 nS.

2-18 GHz HEMT MMIC

A wideband distributed amplifier MMIC was designed to operate across the 2-18 GHz bandwidth. The design of the amplifier was based on an existing 0.25×150 micron HEMT, four of which were used in this circuit. The gate

Table 1: Summary of HEMT LNA Measurements

Device #	Frequency = 9 GHz		Frequency = 10 GHz	
	Gain (dB)	NF (dB)	Gain (dB)	NF (dB)
1	14.2	1.45	11.5	1.65
2	14.0	1.50	11.0	1.75
3	17.6	1.30	15.0	1.20
4	16.0	1.35	13.0	1.50
5	14.3	1.35	11.5	1.60

line design was based on a constant K low pass filter model with uniform transmission line sections. For the 150 micron wide device, the transmission line lengths were adjusted to obtain a nominal 50 ohm filter impedance and cut-off frequency of approximately 20 GHz. The output line was also designed with uniform transmission lines and contained the usual peaking line between the drain of the device and the through drain line.

The amplifier circuit, shown in Figure 3, uses a 0.25 micron HEMT process that incorporates MIM capacitors, thin film resistors, ground vias and is 0.078 in. wide, 0.113 in. long and 0.004 in. thick.

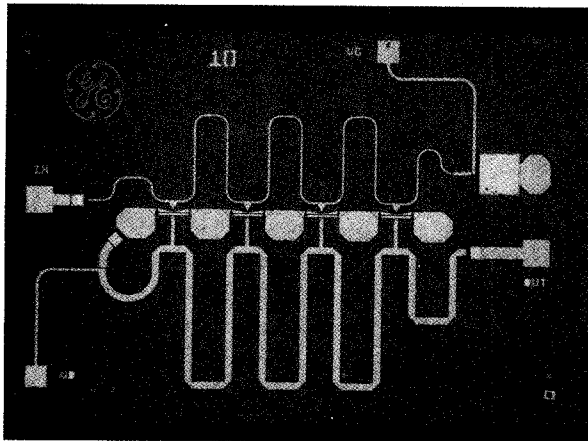


Figure 3. Distributed 2-18 GHz HEMT MMIC. (Chip size: 0.078 x 0.113 in².)

The measured performance, shown in Figure 4, indicates a measured noise figure of less than 3.5 dB across 3-14 GHz and less than 5.2 dB from 2-18 GHz. The gain across the 2-18 GHz bandwidth was 11±0.8 dB, at the same bias point.

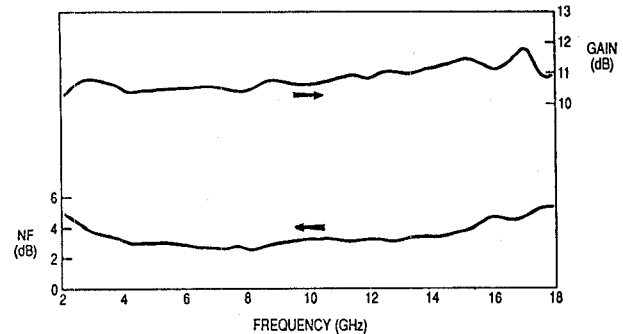


Figure 4. Measured Performance of 2-18 GHz HEMT MMIC

The input and output return losses of this circuit are better than 15 dB up to 15 GHz and 7 dB at 18 GHz.

20 GHz HEMT MMIC

A three-stage 20 GHz HEMT MMIC, shown in Figure 5, was designed to operate across the 20.2-21.2 GHz bandwidth proposed for several military communications systems.

A single-ended circuit topology was used for the amplifier, using matching networks optimized for flat gain and noise figure across the band. The circuit uses three 0.25 x 150 micron HEMT

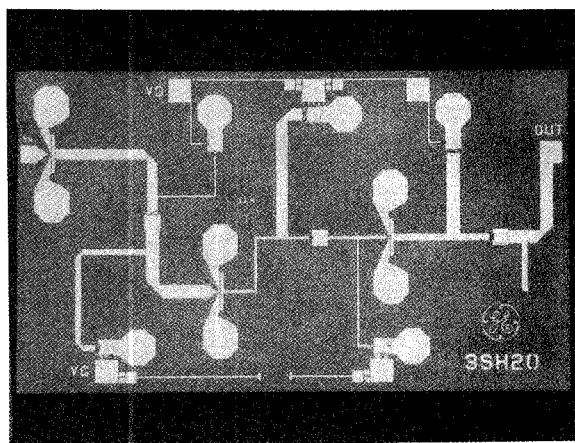


Figure 5. Three-Stage 20 GHz HEMT MMIC.
(Chip size: 0.050 x 0.089 in².)

devices to achieve almost 30 dB of gain. The input matching network was designed on an external 0.010 in. low-loss fused silica substrate. By doing this, it is estimated that the noise figure is improved by approximately 0.3-0.5 dB over on-chip matching, and it allows for tuning on the input substrate to further optimize the noise figure. On the MMIC, the drain bias for the three devices is applied to a common point and similarly the second- and third-stage gate biases are connected together, separated by a 2000 ohm isolation resistor. The gate bias for the first device is applied through the off-chip matching network and optimized for low-noise performance independent of the second and third stages.

The 20 GHz MMIC was fabricated using the same 0.25 micron HEMT process as for the 2-18 GHz MMIC incorporating MIM capacitors, thin film resistors, and ground vias. Circuit size is 0.050 in. wide, 0.089 in. long and 0.004 in. thick.

The measured performance, shown in Figure 6, indicates a measured noise figure of less than 2.0 dB from 18-23 GHz with approximately 29 dB gain. The measured noise figure is for the total amplifier, including the input network and its DC block which uses parallel coupled lines. This represents the highest level of performance yet reported for a low-noise MMIC.

CIRCUIT FABRICATION

All the MMICs were fabricated with selectively doped AlGaAs/GaAs heterostructures grown on undoped GaAs substrates. The material was

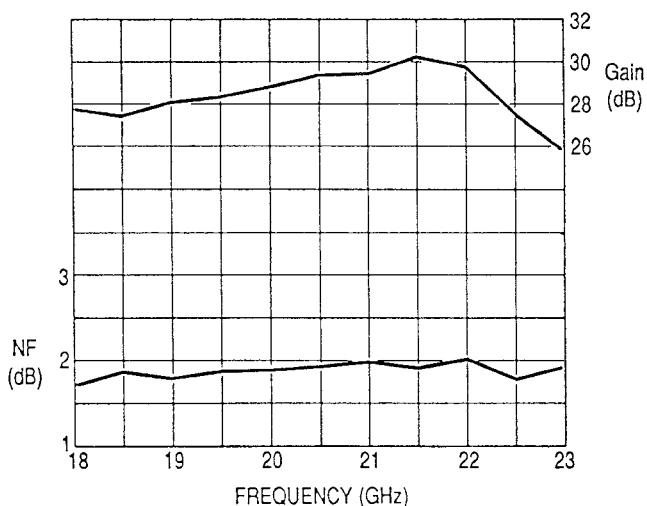


Figure 6. Measured Performance of 20 GHz HEMT MMIC

grown using a Varian GEN II molecular beam epitaxy system at GE. The epitaxial layers consisted of a 1 micron-thick undoped GaAs buffer layer, a 50 Å-thick AlGaAs spacer layer, a 450 Å doped AlGaAs layer, and a 300 Å doped GaAs contact layer. An aluminum composition of 23% was used for all the layers reported in this work. At 77 K, Hall effect measurements yielded a mobility greater than 70,000 cm²/V-s and a sheet carrier concentration of 8.0-9.0x10¹¹ cm⁻².

A hybrid lithographic process was used to fabricate the X-Band HEMT MMIC on 2-inch diameter wafers. An optical stepper was utilized for all lithographic steps except the 0.5 micron gate footprint, which was exposed by a direct-write electron beam system. This lithographic process scheme will lead to affordable HEMT MMICs because it has the potential for higher circuit yields and has higher wafer throughput than an all direct-write process.

Our 0.5 micron process also features a large cross-section T-shaped gate to minimize the parasitic gate resistance. A typical 0.5 micron gate with Ti/Pt/Au layers, shows a gate resistance of only 12Ω/mm. The circuits are passivated with 1550 Å of Si₃N₄ during the formation of MIM capacitors.

In the 0.25 micron process, all lithographic steps, except the airbridge and via-hole levels, were performed on the electron-beam direct writing system to yield good mask registration and 0.25

micron gate finger definition. A tri-layer PMMA/PMAA E-beam resist system was used to form the mushroom-shaped gate. The circuits are passivated with 1000 Å of silicon nitride during the formation of MIM capacitors.

CONCLUSION

In addition to their outstanding low-noise performance, these three circuits, more importantly, represent the rapidly maturing capability of HEMT-based MMIC technology. With the X-Band MMIC a fabrication procedure has been demonstrated that will lead to affordable, high performance HEMT MMICs using a combined optical stepper/E-beam lithographic process.

The current state-of-the-art in reported HEMT MMICs indicates that in the future we can expect HEMT MMICs to outperform FET-based MMICs at all frequencies, especially above 30 GHz. Future radar, EW and communications systems stand to gain significantly from the superior performance of monolithic HEMT LNAs. At EHF frequencies, the HEMT MMIC will become even more crucial for delivering the required performance that, in turn will have a direct impact on also lowering system costs through reduced size, weight, control complexity, and improved reliability.

The experience gained during the design of these HEMT MMICs supports the superiority of HEMTs over FETs in both gain and noise bandwidths as well. The noise figure of a HEMT is not only lower than a comparable FET, but it is also lower over a much larger frequency range and source impedance range, leading to designs that are less sensitive to device and circuit impedance variations. These properties make the HEMT the device of choice for any low noise application.

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REFERENCES

- [1] J.G. Tenedorio, J.J. Komiak, "GaAs MMICs Satisfy EW Requirements," Microwaves & RF (November 1988), vol. 27, no. 12.
- [2] J.F. McIlvenna, "Monolithic Phased Arrays for EHF Communications Applications " Microwave Journal (March 1988), vol. 31, No. 3, pp. 113-125.
- [3] W.H. Perkins and T.A. Midford, "MMIC Technology: Better Performance at Affordable Cost," Microwave Journal (April 1988), vol. 31, No. 4, pp. 135-143.
- [4] D. Hampel, M.A.G. Upton, "GaAs MMICs for EHF SATCOM Ground Terminals," MILCOM 1988, San Diego, CA (October 1988), Paper 42.3.
- [5] C. Yuen, M. Riazat, S. Bandy, G. Zdasiuk, "Application of HEMT Devices to MMICs," Microwave Journal, (August 1988), vol. 31, No. 8, pp. 87-104.
- [6] J. Berenz, H.C. Yen, R. Esfandiari, K. Nakano, T. Sato, J. Velebir, and K. Ip, "44 GHz Monolithic Low Noise Amplifier," 1987 IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium, Las Vegas, NV (June 1987) pp. 15-18.
- [7] N. Ayaki, A. Inoue, T. Katoh, M. Komaru, M. Noda, M. Kobiki, "A 12 GHz- Band Monolithic HEMT Low-Noise Amplifier, " 1988 GaAs IC Symposium, (November 1988) Paper 4.2, pp. 101-104.
- [8] A.F. Podell, "A Functional GaAs FET Noise Model," IEEE Trans. Electron Devices, vol. ED-28, No. 5, pp. 511-517, May 1981.